F1TDC – Preliminary Tests

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Several pictures of the F1TDC board are shown below.

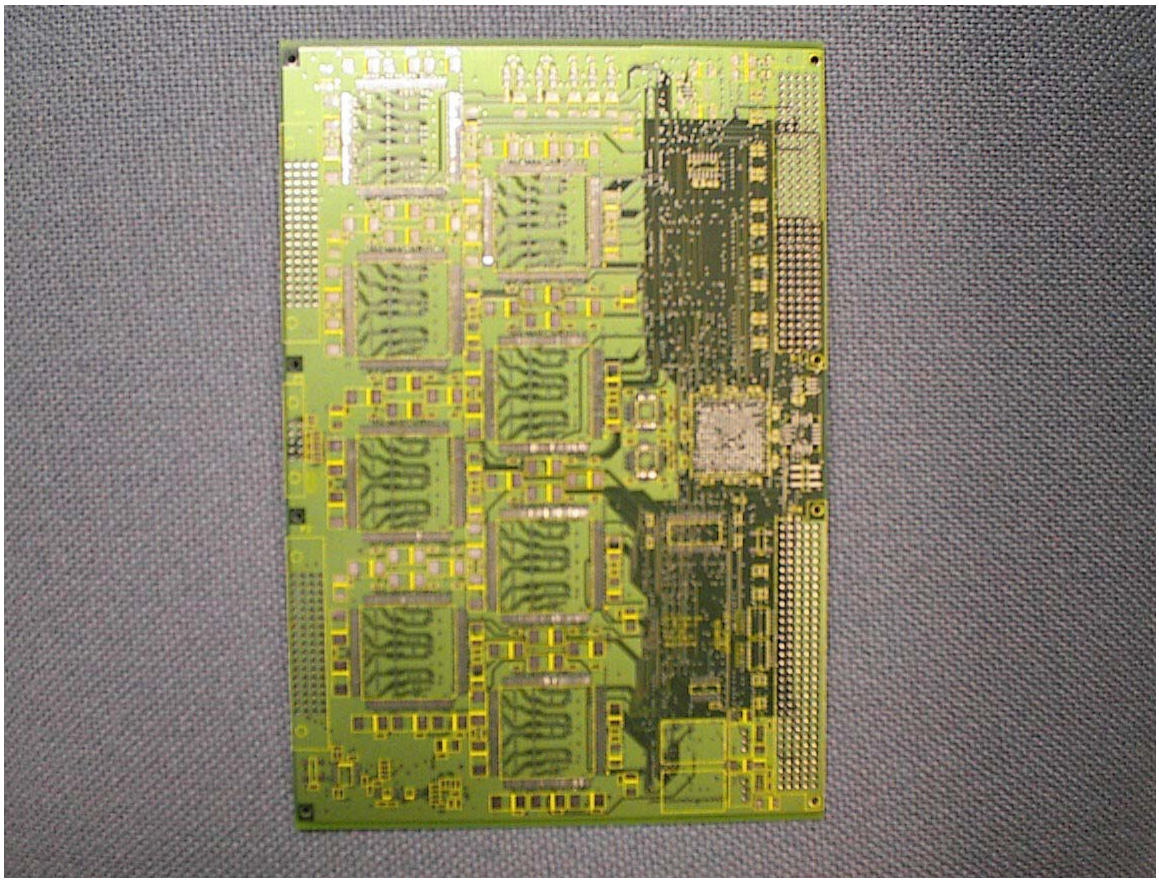


Figure 1 – F1TDC front view

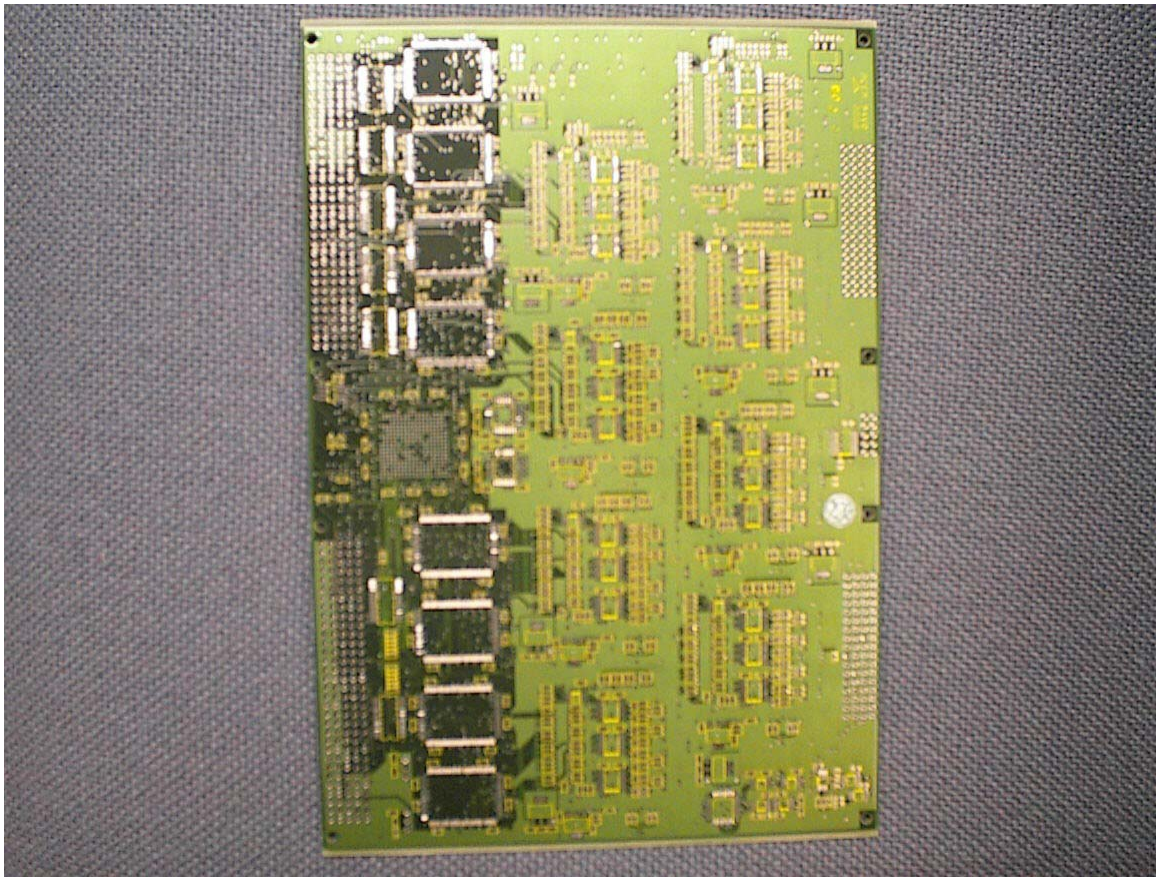


Figure 2 – F1TDC back view

The pictures and waveforms shown below reflect tests of some functions on the front end section. No F1s and the VME interface are not installed.

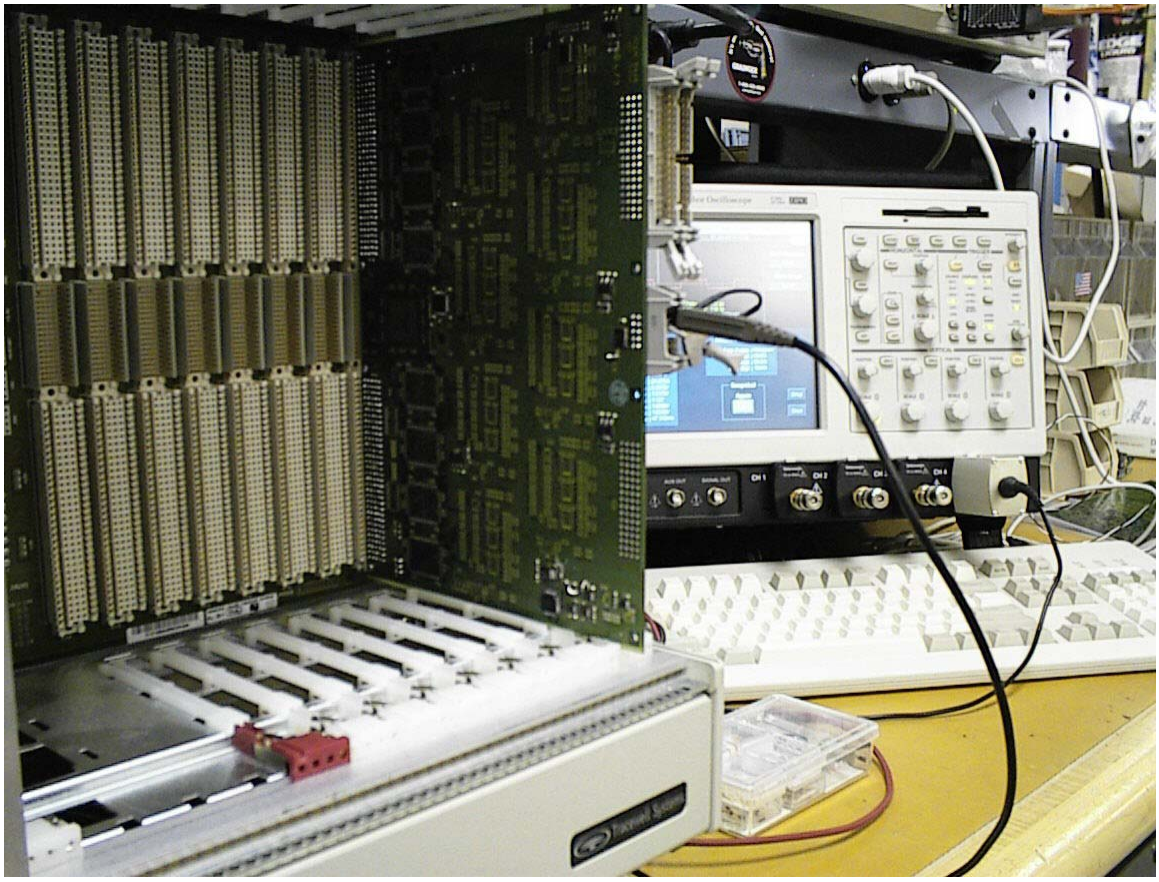


Figure 3 – First tests of the F1TDC

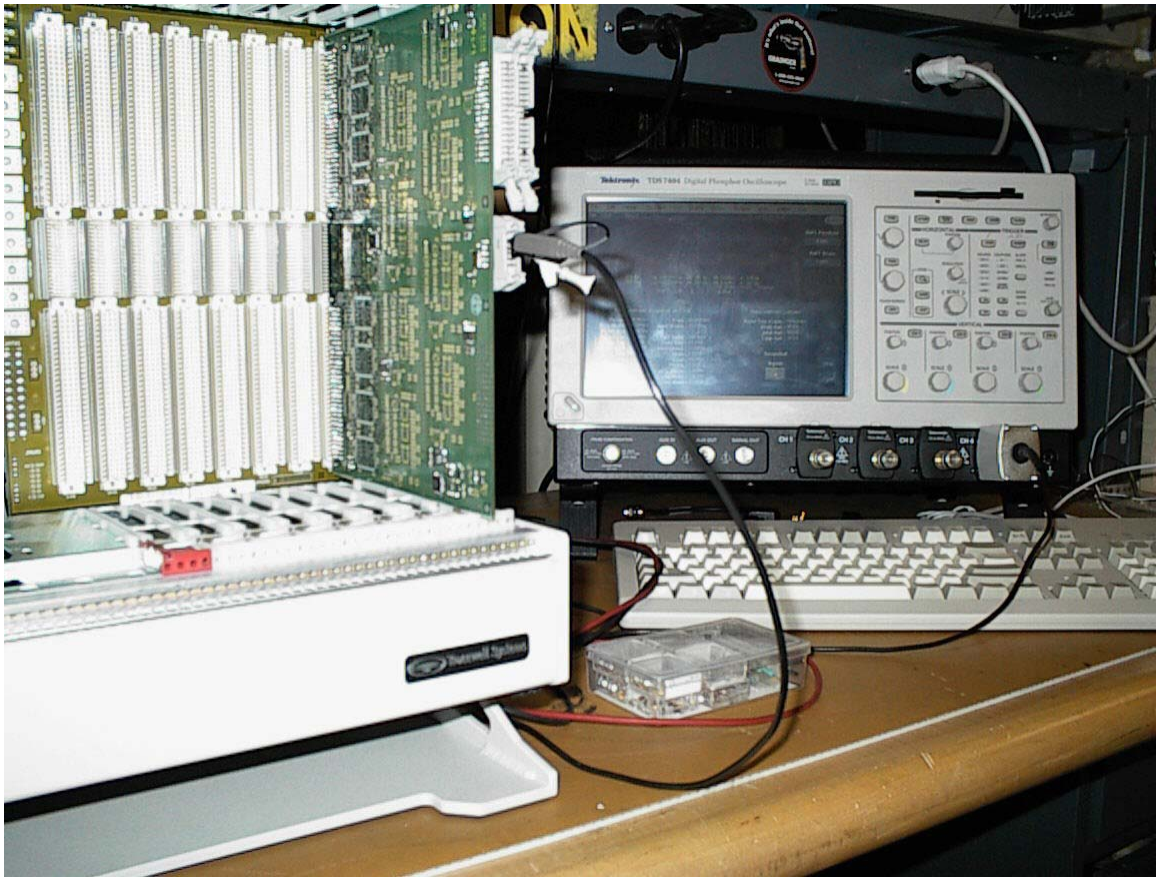


Figure 4 – Another view of the F1TDC under preliminary tests

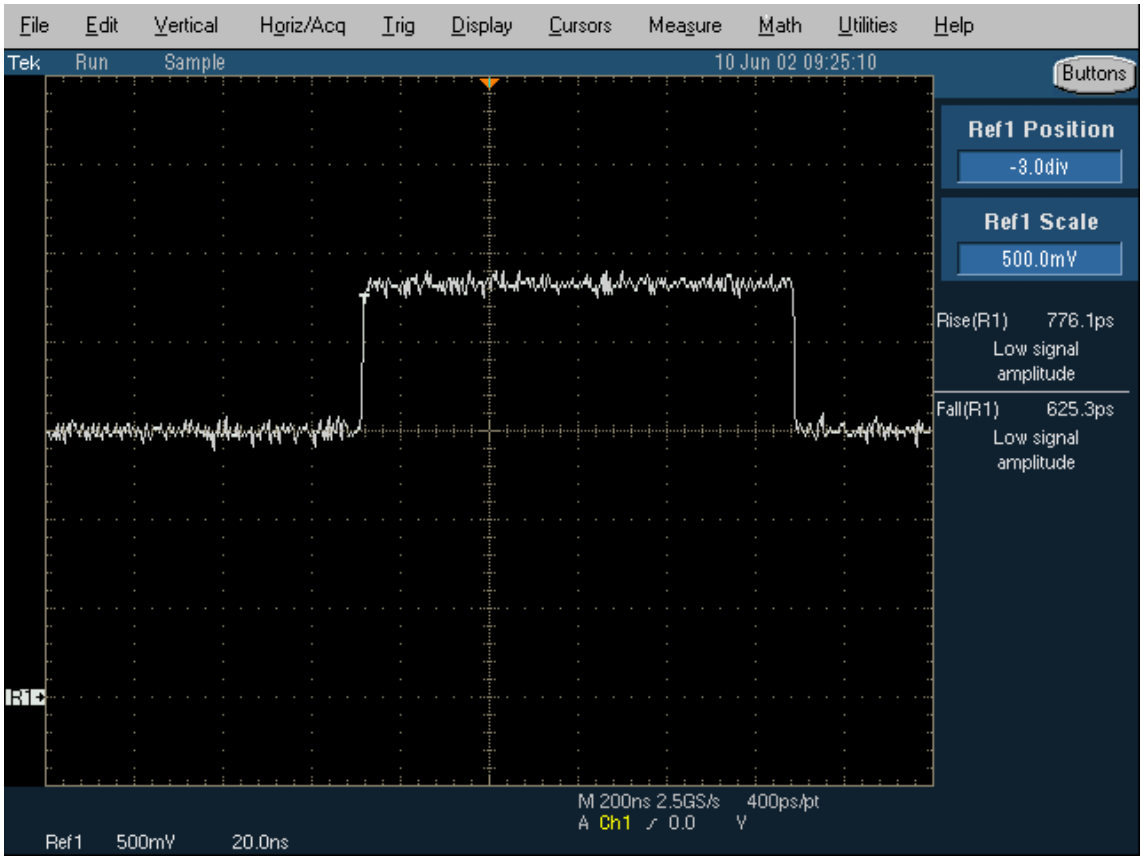
Figure 5 shows the REFCLK+ signal before distribution to the F1 chips. This signal is in PECL and fixed at 40 MHz which will provide 60 pS LSB resolution on the F1s. The REFCLK- signal has similar characteristics. Note the absence of reflections showing correct transmission and termination characteristics. Also note the fast edges. Jitter of this clock signal was determined to be less than 20 pS rms.

Figure 5 – The REFCLK in PECL before distribution to F1 chips

Figure 6 shows the REFCLK+ signal after distribution (also in PECL). This one is at the first F1 chip (F1_1) pad and denoted REFCLK+_1. The signal has traveled about 7 inches through inner board layers designed for a nominal impedance of 50 Ohm. The length of these traces to all F1 chips are of equal length. Note the absence of reflections and fast edges.

Figure 6 – REFCLK+ at the first F1 chip.

Figure 7 shows the result of another important test. This is signal is the STOP+_1 input to the first F1 chip (also PECL). This test consisted of running a NIM pulse (30 ft) to a NIM-to-ECL converter and then fed to the F1TDC trough a 100 ft of twisted pair cable. The input of the F1TDC converts the differential ECL signal to differential PECL and routes the signal to the proper F1 chip pad. Note the absence of reflections and the fast edges. No crosstalk to the adjacent channel was observed.



F1TDC Test Summary

Mechanical	**ok**
Power Distribution	**ok** (resistor added to +1.3V for load regulation)
Clock Generation	**ok**
Input ECL-PECL	**ok**
Signal distribution	**ok**
Plane Impedance	**ok**

Additional tests are in progress.